IN THE CLAIMS:

A detailed listing of all claims that are, or were, in the application follows:

1. (cancelled): A system for displaying visual information, comprising:

a display element;

said display element having means of retaining an array element address;

said display element having means of comparing said address with a received signal;

said display element adapted to extract a display setting upon finding an address match;

said display element adapted to provide a display output according to the extracted display setting;

a display element controller;

said display element controller adapted to generate a signal to a plurality of connected said display elements; and

said display element controller adapted to generate a signal containing a sequence of display settings in an ordered pattern consistent with the addressing of said array elements.

2. (cancelled): A system as recited in claim 1, wherein the means for retaining an array element address comprises cells of a non-volatile memory.

3. (cancelled): A system as recited in claim 1, wherein the means of comparing

address comprises a comparator which compares the present address within the received signal to an address retained within the display element.

4. (currently amended): A display element configured for use in a display array ~~which receives at least one display signal containing a series of display setting values for the elements within the array~~, comprising:

a single input configured for receiving a serial display signal containing a sequence of display setting values and at least one position clocking signal;

a memory ~~digital circuit~~ for retaining an address value;

an address comparison circuit configured for comparing the retained address value with a count of said clocking signal to detect an address match ~~the received signal~~;

a [[an]] data store which extracts a display setting value from the display signal upon [[an]] said address match being detected; and

a visual output element whose optical state ~~which~~ is set in response to the extracted display setting.

5. (currently amended): A display element as recited in claim 4, wherein said single input on said display element is configured to receive said display signal in parallel with a plurality of other display elements ~~controller for the display element recited in claim 4~~.

6. (cancelled): A method of driving display elements, comprising:

generating a display signal containing a series of display settings in a pattern from which a display element address may be determined;

transmitting said signal to an array of synchronous display element;

receiving said signal within a synchronous display element;

detecting an address match for the display element within the signal;

extracting the display setting from the signal for the display element; and

outputting a display setting in response to the extracted display setting.

7. (original): A method of programming an array address within an element of an array, comprising:

configuring display elements with an optical detector;

configuring display elements with a non-volatile section of memory for retaining an address;

optically coupling a programming array to the array of display elements;

engaging the address programming for the displaying elements; and

loading the address embedded within the signal in response to the detection of sufficient light input.

8. (cancelled): A display array having a plurality of multiple display elements which are individually addressable by an attached controller, comprising:

(a) an array support member configured with power and ground connections;

(b) a controller operatively coupled to the power and ground connections of said array support member and capable of applying a voltage between the power and

ground connections, wherein the controller is further capable of superimposing data signals on said voltage; and

(c) a plurality of display elements operatively connected to the power and ground of said support member, each display element being configured to extract the data signals from the voltage provided by the controller, wherein a display element, such as an LED or incandescent element, is activated according to the data if the address of the data matches that of the display element.

9. (new): A display element as recited in claim 4, wherein said visual output element comprises one light emitting diode (LED) of a desired color, or multiple LEDs of at least one color.

10. (new): A display element as recited in claim 4, wherein said single input is configured for receiving said serial display signal over a single signal line coupled directed to each said display element within a given display array, or a signal superimposed on the power being supplied to each said display element within said given display array.

11. (new): A display element as recited in claim 4, wherein said display setting values comprise bits for setting an intensity level and/or color for said visual output element.

12. (new): A display element as recited in claim 4, wherein each given cycle of said display signal includes a predetermined number of data bits for each display element position within a display array.

13. (new): A display element as recited in claim 4, wherein said address comparison circuit is configured with at least one counter which is clocked by said at least one position clocking signal to advance a position address being compared against said address value retained in memory.

14. (new): A display element as recited in claim 4, wherein said position clocking signal comprises a clock which separates display setting values to be displayed along a first dimension of an associated display, and an optional clock for advancing output of said display setting values along a second dimension of said display.

15. (new): A display element as recited in claim 4, further comprising:

means for programming an address into said memory corresponding to the position of said display element within in an array of said display elements.

16. (new): A display element having internal optical output control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

an input configured for receiving an array position addressing signal containing array position clocking and data which are delivered in common to all said display elements within a single or multidimensional display array;

a counter configured for maintaining an array position count in response to detecting said array position clocking from said input;

a memory configured for retaining an array position;

a comparison circuit configured for generating a data load signal in response to detecting a desired relationship between said array position maintained by said counter and said array position retained in said memory;

a latch circuit configured for loading data from said input in response to receipt of said data load signal; and

a driver circuit configured for outputting said data to update the optical state of said at least one optical element.

17. (new): A display element as recited in claim 16, wherein said input comprises a single signal line coupled directed to each said display element within a given display array, or a signal superimposed on the power being supplied to each said display element within said given display array.

18. (new): A display element as recited in claim 16, further comprising:

a shift register coupled to said input and configured to receive data bits of said array position addressing signal in response to said data load signal;

wherein said shift register is configured to output, in parallel, the data bits it has

received to said latch.

19. (new): A display element as recited in claim 16, wherein said memory comprises a non-volatile memory.

20. (new): A display element as recited in claim 19, wherein said memory is configured for being loaded with a array position value in response to a position programming operation.

21. (new): A display element as recited in claim 16, wherein said input comprises a separate signal connection aside from the power and ground connections of said display element.

22. (new): A display element as recited in claim 16, wherein said input is received as a signal superimposed over said power and ground connections to said display element.

23. (new): A display element as recited in claim 16, wherein said array position clocking and data are received for each array address in each cycle of an array position addressing signal.

24. (new): A display element as recited in claim 23, wherein said driver is configured for outputting said data to said at least one optical element in response to

detecting the end of said cycle of said array position addressing signal.

25. (new): A display element as recited in claim 16, wherein said driver circuit is configured for modulating the optical state of each of said optical elements to either an on or off state in response to said data from said latch circuit.

26. (new): A display element as recited in claim 16, wherein said driver circuit is configured for modulating the optical state of each of said optical elements to a desired intensity and/or color in response to said data from said latch circuit.

27. (new): A display element having an integral optical state output control circuit, comprising:

at least one optical element configured for displaying multiple optical states;

means for modulating the optical state of said at least one optical element in response to data extracted at a programmed address position within a cycle of an array position addressing signal which supplies serial data to be commonly received in parallel by a plurality of said display elements; and

an optical housing containing said at least one optical element coupled to said modulating means, said optical housing configured with a transparent portion through which the state of said at least one optical element may be viewed.

28. (new): A display element as recited in claim 27, wherein said means for modulating the optical state is configured for modulating each of said at least one

optical element into a state of either on or off.

29. (new): A display element as recited in claim 27, wherein said means for modulating the optical state is configured for modulating the intensity and/or color for each of said at least one optical element.

30. (new): A display element as recited in claim 29, wherein said intensity is controlled by an analog or digital intensity control mechanism.

31. (new): A display element as recited in claim 27, wherein said modulating means is configured for modulating the optical state of said at least one optical element within said display element in response to an array position addressing signal being commonly received by a single axis or multiple axis array of optical elements.

32. (new): A display element as recited in claim 27, wherein said programmed address position within a cycle of said array position addressing signal from which data is extracted is determined in response to the value of an array address programmed into non-volatile memory within said display element.

33. (new): A display element as recited in claim 27, wherein said array address may comprise one or more axis of addressing.

34. (new): A display element as recited in claim 33, wherein said array address comprises a row address and a column address.

35. (new): A display element as recited in claim 27, wherein said array position addressing signal comprises a predetermined number of data bits for each given position within a cycle of said array position addressing signal.

36. (new): A display element as recited in claim 27, wherein the optical state of said at least one optical element is updated from previously extracted data at a fixed position within said array position addressing signal, whereby the optical state of all display elements in an array which are coupled to said array position addressing signal change at the same time.

37. (new): A display element as recited in claim 36, wherein said fixed position occurs at the end of a cycle of said array position addressing signal.

38. (new): A display element as recited in claim 27, wherein said optical element comprises one light emitting diode (LED) of a desired color, or multiple LEDs of at least one color.

39. (new): A display element as recited in claim 27, wherein said optical element and said modulating means are contained on the same integrated circuit die.

40. (new): A display element as recited in claim 27, wherein said optical element and said means for modulating the optical state are contained on at least two integrated circuit die which are coupled to one another and retained in said optical housing.

41. (new): A display element as recited in claim 27, wherein said modulating means comprises:

a memory configured for being programmed to the address for the position of said display element within an array of display elements;

a counter configured for counting clocks to maintain a current address within said array position addressing signal;

an address comparator for generating a matching signal in response to detecting a predetermined relationship between said current address maintained by said counter and the address within said memory;

a data store configured for collected data bits from said array position addressing signal in response to said matching signal; and

a driver circuit configured for modulating the state of said at least one optical element in response to said collected data bits.

42. (new): A display element as recited in claim 27, further comprising:

means for detecting a programming signal while said display element is in a programming mode; and

means for programming the position within said cycle of an array position

addressing signal at which said data is extracted in response to the detection of said programming signal by said programming signal detection means.

43. (new): A display element as recited in claim 42, wherein said means for programming comprises:

a non-volatile memory configured for retaining information about the position within said cycle; and

a circuit for loading a counter value, which is tracking said position within said cycle of an array position address signal, into said non-volatile memory in response to detecting said programming signal while said non-volatile memory is in a programming state.

44. (new): A display element as recited in claim 27, wherein said modulation means is configured for receiving clocking and data signals of said array position addressing signal over a single input or superimposed on the power connections supplying power to said display element.

45. (new): A display element as recited in claim 44:

wherein said display element is configured for being coupled to a power and ground line, or plane, with other display elements within a display array;

wherein said display element draws power from said power and ground line or plane;

wherein said display element is configured for receiving said array position

addressing signal from said power and ground line or plane.

46. (new): A display element as recited in claim 27:

wherein said array position addressing signal comprises a sequence of data configured for receipt by sequentially addressed display elements and a clock which separates the data for extraction at each programmed address position; and

wherein optional clocks can be contained within said array position addressing signal for advancing output of said display setting values along an additional display axis.

47. (new): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for programming to a first address associated with the position of said display element within an array of said display elements;

means for extracting output data from a data signal, received in parallel by the display element and other display elements within an array of display elements, in response to matching a second address received on said data signal with said first address; and

means for modulating the output of said at least one optical element in response to said extracted output data.

48. (new): A display element as recited in claim 47, wherein said first address comprises at least one axis of addressing.

49. (new): A display element as recited in claim 48, wherein said first address comprises a row and column address.

50. (new): A display element as recited in claim 47, wherein said means for extracting data is configured for extracting a predetermined number of data bits from said data signal.

51. (new): A display element as recited in claim 50, wherein said means for extracting data is configured for counting clocks on said data signal for determining said second address.

52. (new): A display element as recited in claim 51, wherein said clocks comprise column and row clocks.

53 (new): A display element as recited in claim 51, wherein said means for extracting data is configured for detecting a reset clock to reset the clocks being counted in determining said second address.

54. (new): A display element as recited in claim 47, wherein said data signal signal comprises either a single signal line coupled directed to each said display

element within a given array of said display elements, or is superimposed on the power being supplied to each said display element within the array of display elements.

55. (new): A display element as recited in claim 47, wherein said means for modulating the output of the optical state of said at least one optical element is configured to update the optical state of said optical element at a fixed position within cycles of said data signal.

56. (new): A display element as recited in claim 55, wherein said fixed position occurs at the end of a cycle of said data signal.

57. (new): A display element as recited in claim 47, wherein said means for extracting data from said common array positioning addressing signal, comprises:

a counter configured for counting clocks to determine said second address within said data signal;

an address comparator for generating a matching signal in response to detecting a predetermined relationship between said second address determined by said counter and said first address retained within said memory; and

a data store configured for collecting data bits from said data signal in response to said matching signal.

58. (new): A display element as recited in claim 47, wherein said modulating means comprises:

a latch configured for latching and outputting data bits from said data store; and

a driver circuit configured for driving said at least one optical element to provide intensity and/or color control in response to output data being output from said latch.

59. (new): A display element as recited in claim 58, wherein said latch is configured to output the received data in response to a predetermined position within each cycle of the data signal.

60. (new): A display element as recited in claim 47, wherein said optical element comprises one light emitting diode (LED) of a desired color, or multiple LEDs of at least one color.

61. (new): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for storing a first address for the display element;

means for extracting output control data from a data signal, received in parallel with other display elements within an array of the display elements, in response to matching a second address received from the data signal with said first address; and

means for modulating the output state of at least one said optical element in response to said extracted output control data.

62. (new): A display element as recited in claim 61, further comprising means for programming said memory to said first address in response to the position of the display element within an array of the display elements.

63. (new): A display element as recited in claim 62, wherein said programming means is configured for loading said second address from the data signal in response to a programming signal received by said display element and not by other display elements within an array which are not to respond to given said second address.

64. (new): A display element as recited in claim 63, wherein said programming means is configured to program said second address in response to a combination of data received from said data signal and said programming signal.

65. (new): A display element as recited in claim 63, further comprising an optical detector within said display element, said optical detector configured for receiving said programming signal.

66. (new): A display element as recited in claim 65, wherein said optical detector comprises one or more of said at least one optical elements which are configured for both displaying optical states and detecting optical input.

67. (new): A display element as recited in claim 66, wherein said optical detector comprises at least one separate optical input sensor integrated within said

display element.

68. (new): A display element as recited in claim 61, wherein said output control data is received on the data signal in a sequential scan form or random form.

69. (new): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for storing a first address for the display element in response to the position of the display element containing said at least one optical element within an array of said display elements;

means for extracting output control data from a common data signal received in parallel with other display elements within an array of the data elements, said output control data being extracted in response to detecting a desired relationship between said first address stored in memory and a second address received over said common data signal; and

means for modulating the output of at least one said optical element in response to said extracted output control data.

70. (new): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

means for outputting optical state data, received from a data signal, to said at

least one optical element in response to matching a first address received from the data signal with a second address programmed within said means to the position of the display element within an array of the display elements.

71. (new): A display element as recited in claim 70, wherein said outputting means is configured for programming said second address in-situ.

72. (new): A display element as recited in claim 70, wherein said outputting means is configured for receiving said data signal in parallel with other display elements within the array of display elements.

73. (new): A display element as recited in claim 70, wherein said second address is programmed into non-volatile memory within said outputting means.

74. (new): A method of controlling a display element, comprising the steps of:

programming a memory within a display element to a first address corresponding to the position of the display element within an array of other display elements;

detecting a match between said first address and a second address contained within a data signal that is received in parallel by display elements within the array;

loading a predetermined number of bits of display data from the data signal in response to said match; and

outputting said number of bits to a optical element driver which controls the intensity and/or color of at least one optical element within the display element in

response to said bits.

75. (new): A method as recited in claim 74, wherein said data signal is extracted from a two lead power bus coupled to the display element on which the data signal has been superimposed for receipt by the display element.

76. (new): A method as recited in claim 74, wherein the at least one optical element comprises one light emitting diode (LED) of a desired color, or multiple LEDs of at least one color.